

Amendments to the Claims:

Claim 1. (Previously Presented) A method for in-place memory management in a Digital Signal Processing (DSP) architecture performing a Fast Fourier Transformation (FFT) upon a sequence of  $N$  data points, said sequence numbered from 0 to  $N-1$ , the method comprising:

storing each of said data points numbered from 0 to  $(N/2)-1$  in a first memory space X and each of said data points numbered  $N/2$  to  $N-1$  in a second memory space Y; and

for each FFT stage 0 data point grouping comprising a first data point of said data points in said first memory space X and a corresponding second data point of said data points in said second memory space Y:

determining a parity of a data point memory index corresponding to said first and second data points;

storing, if said parity is of a first parity value, the results of an FFT operation upon said first data point at the memory address in said first memory space X from which said first data point was fetched and the result of an FFT operation upon said second data point at the memory address in said second memory space Y from which said second data point was fetched; and

storing, if said parity is of a second parity value, the results of an FFT operation upon said first data point at the memory address in said second memory space Y from which said second data point was fetched and the result of an FFT operation upon said second data point at the memory address in said first memory space X from which said first data point was fetched.

Claim 2. (Original) A method according to claim 1 and further comprising:

for any FFT stage Z subsequent to stage 0 and each FFT stage Z data point grouping comprising a first data point in said first memory space X and a corresponding second data point in said second memory space Y, storing the results of an FFT operation upon said first data point at the memory address in said first memory space X from which said first data point was fetched and the results of an FFT operation upon said second data point at the memory address in said second memory space Y from which said second data point was fetched.

APPLICANT(S): Gil VINITZKY  
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Claim 3. (Currently Amended) A method comprising:

determining a parity of a memory index, where a first data point of a pair of input data points of ~~a first~~ an initial stage of a Fast Fourier Transform calculation is stored in a first memory space at a first address corresponding to said memory index and a second data point of said pair is stored in a second memory space at a second address corresponding to said memory index;

if said parity is of a first parity value, storing a first output data point of said ~~first~~ initial stage at said first address in said first memory space and a second output data point of said ~~first~~ initial stage at said second address in said second memory space; and

if said parity is of a second parity value, storing said first output data point at said second address in said second memory space and said second output data point at said first address in said first memory space.

Claim 4. (Currently Amended) The method of claim 3, further comprising:

storing an output data point of ~~said second~~ a subsequent stage that is associated with said first output data point at the address in the memory space where said first output data point was stored; and

storing an output data point of said ~~second~~ subsequent stage that is associated with said second output data point at the address in the memory space where said second output data point was stored.

Claim 5. (Currently Amended) A method comprising:

determining, based at least on a parity of a memory index, whether to store an output data point of ~~a first~~ an initial stage of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address, where a first data point of a pair of input data points of said ~~first~~ initial stage is stored in said first memory space at said first address and a second data point of said pair is stored in said second memory space at said second address, and where said first address and said second address both correspond to said memory index.

Claim 6. (Currently Amended) A digital signal processor comprising:

a first memory space to store a first data point of a pair of input data points of a ~~a~~ **first an initial** stage of a Fast Fourier Transform calculation at a first address corresponding to a memory index;

a second memory space to store a second data point of said pair at a second address corresponding to said memory index; and

means for determining, based at least on a parity of said memory index, whether to store an output data point of said **first initial** stage in said first memory space at said first address or in said second memory space at said second address.

Claim 7. (New) A method comprising:

determining a parity of a memory index, where a first data point of a pair of input data points of a stage of a Fast Fourier Transform calculation is stored in a first memory space at a first address that is the sum of a first base address and said memory index, and a second data point of said pair is stored in a second memory space at a second address that is the sum of a second base address and said memory index;

if said parity is of a first parity value, storing a first output data point of said stage at said first address in said first memory space and a second output data point of said stage at said second address in said second memory space; and

if said parity is of a second parity value, storing said first output data point at said second address in said second memory space and said second output data point at said first address in said first memory space.

Claim 8. (New) A method comprising:

determining, based at least on a parity of a memory index, whether to store an output data point of a stage of a Fast Fourier Transform calculation in a first memory space at a first address or in a second memory space at a second address, where a first data point of a pair of input data points of said stage is stored in said first memory space at said first address and a second data point of said pair is stored in said second memory space at said second address, and where said first address is the sum of a first base address and said memory index and said second address is the sum of a second base address and said memory index.